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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,977	10/07/2003	William R. Dunn	AME1638-005A	4778
	STANDLEY LAW GROUP LLP		EXAMINER	
495 METRO PLACE SOUTH			NGUYEN, THANH NHAN P	
SUITE 210 DUBLIN, OH	43017		ART UNIT	PAPER NUMBER
2022., 0.2 002.			2871	
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			12/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		oH.
	Application No.	Applicant(s)
	10/679,977	DUNN ET AL.
Office Action Summary	Examiner	Art Unit
	(Nancy) Thanh-Nhan P. Nguyen	2871
The MAILING DATE of this communication Period for Reply	appears on the cover sheet with the	correspondence address
A SHORTENED STATUTORY PERIOD FOR RE WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 GFF after SIX (6) MONTHS from the mailing date of this communication If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by standard patent term adjustment. See 37 CFR 1.704(b).	B DATE OF THIS COMMUNICATIO R 1.136(a). In no event, however, may a reply be till riod will apply and will expire SIX (6) MONTHS from atute, cause the application to become ABANDONE	N. mely filed the mailing date of this communication. ED (35 U.S.C. § 133).
Status		
1)⊠ Responsive to communication(s) filed on 2	<u> 5 September 2007</u> .	
	This action is non-final.	
3) Since this application is in condition for allo closed in accordance with the practice under		
Disposition of Claims		
4) ⊠ Claim(s) 2,4,5,7-10,12-14,16 and 18-20 is/a 4a) Of the above claim(s) is/are without 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 2,4,5,7-10,12-14,16 and 18-20 is/a 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and	drawn from consideration. are rejected.	
Application Papers		
9) The specification is objected to by the Exam		
10)⊠ The drawing(s) filed on <u>18 January 2005</u> is/		•
Applicant may not request that any objection to	• • • • • • • • • • • • • • • • • • • •	· ·
Replacement drawing sheet(s) including the cor 11) The oath or declaration is objected to by the		
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of:  1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the p	ents have been received. ents have been received in Applicat	ion No
application from the International Bur		
* See the attached detailed Office action for a	list of the certified copies not receive	∍d.
Attachment(s)		
1) X Notice of References Cited (PTO-892)	4) Interview Summary	/ (PTO-413)
<ul> <li>2) Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3) Information Disclosure Statement(s) (PTO/SB/08)</li> <li>Paper No(s)/Mail Date</li> </ul>		ate

### **DETAILED ACTION**

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al (US 2004/0036834) in view of Terada (US 5247374).

Regarding claims 12-14, Ohnishi et al discloses (fig. 3) a flat panel display comprising:

- a front glass plate (2)
- a rear glass plate (1)
- a layer of liquid crystal (3) interposed between said front and rear glass plates
- a TFT array layer (considering a TFT array layer is a layer with element(s)
   between the rear glass plate and the liquid crystal layer emphasis added)
   interposed between said front and rear glass plates
- a heater layer (8) integral to the TFT array layer between the glass substrates to allow faster heating of the layer of liquid crystal (element '8' could be formed on TFT substrate or on both of the substrates - par. 0087). The heater layer is patterned onto the TFT substrate in the grid form of intersecting horizontal and vertical lines (par. 0036, wherein the heater layer is patterned corresponding to

the display area in a matrix pattern, the display area includes an area where the black matrix is provided).

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Ohnishi et al fails to disclose the heater layer is made of metal instead of the disclosed ITO heater.

However, Terada teaches (col. 3, lines 24-26) that the heater 6 is comprising electric conductive thin films of an indium tin oxide, a gold or the like material (each serving as a heating element). Thus, the use of the metal (at least gold material) and the use of ITO are considered art-recognized equivalent for this purpose.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form a flat panel display as taught by Ohnishi et al wherein the heater layer is made of a metal instead of ITO as taught by Terada since it is recognized in the art that ITO heater layer and metal heater layers are equivalent as evidenced by Terada.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al in view of Terada as discussed above, and further in view of Takasu et al (US 6067062).

Regarding claims 18-20, Ohnishi et al lacks disclosure of at least one thermal sensor integral to said TFT array layer, wherein the at least one thermal sensor is applied onto said TFT array layer and wherein the at least one thermal sensor comprises an array of diodes.

Takasu et al discloses (fig. 28) at least one thermal sensor integral to said TFT array layer to provide temperature sensing of said layer of liquid crystal (par. bridging

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columns 20-21), wherein the at least one thermal sensor is applied onto said TFT array layer (since the sensors are formed at the same time as the TFT used for the pixel array), and wherein the at least one thermal sensor comprises an array of diodes (fig. 27 and first full paragraph of column 20).

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have at least one thermal sensor integral to said TFT array layer, wherein the at least one thermal sensor is applied onto said TFT array layer and wherein the at least one thermal sensor comprises an array of diodes for providing temperature sensing of said layer of liquid crystal.

Claims 16, 2, 4, 5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al in view of Terada as discussed above, and further in view of Taniguchi et al (US 6839104) and Shin et al (US 6417900).

Regarding claim 16, Ohnishi et al lacks disclosure of a black mask EMI layer interposed between said front and rear glass plates and wherein said black mask EMI layer is electrically tied to zero potential and isolated from Vcom.

Taniguchi et al discloses (fig. 20) that the EMI layer is a black mask layer (6) having light shielding properties and electrically isolated from Vcom (24), but Ohnishi et al and Taniguchi et al fails to specify that EMI layer is tied to zero potential.

However, Shin et al teaches (col. 5, lines 45-46) a black matrix layer sets to be a ground potential. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form a display as the one taught by Ohnishi et al with a black mask taught by Taniguchi et al, wherein the black mask is tied

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to zero potential, as taught by Shin et al. With the above-mentioned configuration, it is thus seen that wider viewing angles are obtained by setting the black mask to a ground potential, as taught by Shin et al (col. 9, lines 44-45).

Regarding claims 2 and 8, Ohnishi et al discloses (fig. 3) an insulating dielectric layer (9) interposed between the inside surfaces of said front and rear glass plates, wherein the insulating dielectric over-coated onto the heater layer (par. 0037).

Claim 4 is met the discussion regarding claim 13 rejection above.

Regarding claim 5, Ohnishi et al lacks disclosure of wherein said metal heater layer is behind said black mask EMI layer.

Taniguchi et al discloses (fig. 20) an EMI layer (6) made of a metal, i.e. Cr, which has low electrical resistance with EMI shielding functionality (col. 11, lines 65-66). Since the EMI layer is disposed on the upper glass substrate corresponding to the TFT regions, the metal heater layer is then optically hidden behind the EMI layer.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the EMI layer as taught by Taniguchi et al into the display configuration as taught by Ohnishi et al for preventing the leakage of light and interference, as taught by Taniguchi et al (col. 2, lines 57-59).

Claim 7 is met the discussion regarding claim 14 rejection above.

Claim 9 is met the discussion regarding claim 18 rejection above.

Claim 10 is met the discussion regarding claim 20 rejection above.

# Response to Arguments

Applicant's arguments with respect to claims 2, 4, 5, 7-10, 12-14, 16 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

#### Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6157432.

US 5559614.

US 4634225.

US 4593978.

#### **Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen Examiner Art Unit 2871

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Supervisory Patent Examiner Technology Center 2800